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REVIEW OF FAULT IDENTIFICATION USING OF NN BASED GA PARAMETERS IN ANALOG CIRCUITS

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Abstract

Fault analysis in analog circuits has been a subject of research for the last few decades because of the complexity in identifies defect models. This paper proposes a fault identify an approach for analog circuits using hybrid evolutionary techniques and neural networks. A neural network is used because of its good robustness and adaptability and a genetic algorithm is used as an evolutionary technique for optimizing and learning neural networks. The proposed method is validated through a state-variable filter circuit and takes all possible parametric variations for faulty and non-faulty conditions and experimental results are presented to show that the comparison of the hybrid scheme neural network method is more efficient**.**

1. Introduction

This project is about fault detection in analog circuits by using neural network optimized by genetic algorithm. Parametric faults of circuit under test are first analyzed and fault dictionary is prepared. This fault dictionary is utilized to compare the component values with the nominal values for fault classification. Neural network is developed by fault dictionary given as input and target set; weights of this neural network are optimized by genetic algorithm with different parametric conditions. Performance of the network is analyzed for different genetic algorithm parameters and best parametric condition of genetic algorithm is chosen to train the neural network for analog fault detection process.

The artificial neural network-based approach for faulty diagnosis is efficient due to its good learning capability, adaptability, and robustness [3]. A neural network is a reciprocal combination of simple processing elements, units, or nodes, whose functionality is based on the neuron. The processing power of the network is stored in the strength or weight of the relationship between the units, which is achieved through learning or learning a set of

training patterns. There are various types of network topology and learning algorithms to train neural networks for the desired task. Neural networks are used for fault detection in many ways, such as fault detection based on parametric variation of circuit components, fault dictionary based approaches, application of circuit knowledge in domains, and more. All these methods are discussed in this study.

2. Motivation

Analog electronics are used at the edge of the digital world and deal with messy problems like converting light, sound and motion to and from digital signals. They deal with real world problems like power and while they may have digital masters, they do the real work. For some tasks, particularly amplification, analog represents the most elegant, direct, and accurate way to perform the task. While Conversion to and from the digital domain also can't beat a properly-designed analog circuit. The rise of system-on chip (SOC) technology has also dramatically boosted the importance of analog circuitry, moving it more into mainstream integrated circuit (IC) design. Analog and digital circuits are now being integrated into a SOC, a mixed-signal system on chip circuits can be a combination of analog circuits and digital circuits. It is reported that 80% of the faults occur in the analog segments in mixed signal circuits [19]. Thus a novel fault detection method for various applications of analog circuits using neural network and genetic algorithm is proposed in this project.

3. Related work

Ashwani Kumar Narula and Amar Partap Singh (2015) presented a paper titled as “Fault Identification of Mixed-Signal Analog Circuit using Artificial Neural Networks”, in this method parametric fault identification of mixed signal analog circuit using neural network is presented. A benchmark R2R digital to analog circuit has been used as CUT for experimental validations. Methodology is categorised as circuit response measurement, fault classification and development of virtual instrument. Measurement of circuit response is done by simulating the circuit with MULTISIM software to get the simulated data and in real time the data is collected from data acquisition system of NIELVIS II board. Input data required for fault identification process is collected by analysing the response data using sensitivity analysis of the CUT. Fault models are taken by parametric variation of ±50% in the resistance value of CUT. Parametric behaviour of component is checked by performing 50 runs of Monte-Carlo analysis. Sensitivity of all resistance is calculated for

each run of all the defined faults. Sensitivity analysis gives the optimum number of input combinations required for fault identification . These input combinations are applied for each Monte-Carlo run of each defined fault model to get the output response of CUT. Fault classification is done by preparing fault dictionary and then the design of the artificial neural network. Fault dictionary is prepared by taking output responses for the different fault models. Total number of fault models, output responses and number of Monte-Carlo run decides the size of the fault dictionary. Multilayer artificial neural network (ANN) is designed in which input layer neurons are equal to number of output responses obtained from optimum number of inputs and number of output layer neurons are equal to number of fault models including non-faulty state of CUT. ANN is trained by using error back propagation training algorithm. Mean square error (MSE) has been taken as performance metric for artificial neural network. ANN is designed in MATLAB software. Virtual instrument is designed in LABVIEW software which contains a block diagram involving graphical code of fault identification system and a front panel which contains displays of input, output and fault indicators and thus we get the fault in the display section. Novelty of this method is that it has been generalised by validating simulated as well as real time data [3].

Mohd Ayub Khan, Divya Rawat, Mahima Singh, Meghna Acharya, Monika Garg (2015) presented a paper titled as ”FAULT DETECTION IN ANALOG CIRCUIT USING NEURAL NETWORK”, in this method neural network based fault detection in analog circuit using transient response of the circuit is presented. This method is experimentally validated through Tuned Amplifier circuit. Data for training and testing set for neural network is collected from Pspice and MULTISIM simulator. Input voltage is kept fixed at 5V and output is taken by varying the frequency. Output of fault free circuit after simulation is compared with output of faulty circuit for detection of fault in circuit. Neural network is designed by using MATLAB software for fault identification . It is a basic neural based method for fault detection and thus it may have poor performance and time constraint [4].

Prithviraj Kabisatpathy, Alok Barua, and Satyabroto Sinha (2004), presented a paper titled as “Fault Detection and Identification in Analog Integrated Circuits Using Artificial Neural Network in a Pseudorandom Testing Scheme”, a different method for fault detection and identification in analog integrated circuits using ANN is proposed in this paper. This method uses a pseudorandom testing scheme. The property of the Gaussian white

noise that its auto- correlation is a single Dirac-δ function is exploited in this research. Testing scheme proposed uses a pseudorandom noise as the input stimulus, thereby providing a good estimation of impulse response of CUT. This method utilises a fault model driven testing technique, which requires only simple output response measurement. The basic approach of the identification method is to compare the CUT against the mathematical model of the fault free circuit, implemented using simple multilayer ANN. The procedure of this methodology is divided in three stages: Signature generation, generation of residuals, detection and isolation of faults. CUT is simulated using the pseudo-random noise and the output response of the CUT forms the signature for fault class. For residual generation: nominal, actual and faulty CUT models are required. All the models are created using simple multilayer ANN consisting of one input layer, one or two hidden layer and one output layer. The ANN models are trained using BP algorithm to give the output responses under both faulty and fault free conditions. The difference between outputs of the nominal model and model of the actual CUT generates residual. Any fault in the circuit will change the signature of the residual. These residual signatures of the known fault condition of the circuit is known as fault signatures, these are first simulated and stored in a model bank for future use. Pseudorandom test stimulus provides a natural spread spectrum test signal, the test generation problem is completely eliminated and it can be used as universal stimulus for testing of analog ICs. The efficiency of this testing method relies on the proper choice of signatures and discrimination schemes to distinguish between the fault free and the faulty circuit in the dictionary [4].

Mansour Sheikhan, Amir Ali Sha'bani (2013), presented a paper titled as "PSO-optimized modular neural network trained by OWO-HWO algorithm for fault location in analog circuits". In this study, an active filter circuit is used as the CUT and is simulated in both fault-free and faulty conditions. A modular neural network based method is proposed for soft fault identification of the CUT. To optimize the structure of neural network modules, particle swarm optimization (PSO) algorithm is used to determine the number of hidden layer nodes of neural network modules. Instead of conventional output weight optimization– back-propagation (OWO-BP) algorithm, hidden weight optimization (OWO-HWO) training algorithm is employed to improve convergence speed in training of the neural network module. Experimental results show that the PSO-optimized modular neural network model which is trained by the OWO-HWO algorithm

offers higher correct fault location rate in analog circuit fault identification application as compared to the classic and monolithic investigated neural models [5].

4. Problem Identification

Fault detection in analog circuit is challenging due to poor fault models, limited test nodes, component tolerance, non- linearity of outputs, limited internal nodes, presence of feedback loops and limited access to internal nodes. Ability of neural network to classify fault models makes neural network an efficient tool to identify faults in analog circuits. But neural network has poor generalization ability and requires large number of iterations for the learning process of neural network and also neural network works on predictions so it takes more time to give the best performance of the system. Back propagation neural networks also tend to be slower to train than other types of network and require large number of epochs and had a property of rapid convergence over local optima.

5. Methodology

5.1. Artificial Neural Network

An Artificial Neural Network (ANN) is a parallel, distributed information processing structure consisting of processing units interconnected through unidirectional signal channels called connections. Each processing unit has a single output connection that branches into as many collateral connections as desired. Each connection carries the same signal that is called as processing unit output signal[9]. General model of ANN followed by its processing is shown in Figure 1.2. In the general model of ANN, net input is calculated as:

$$Y_{in} = x1.w1 + x2.w2 + x3.w3 + \cdots \ldots\ldots\ldots xm \times wm \qquad (1.1)$$

$$Y_{in} = \sum xi \times wi \qquad (1.2)$$

The output can be calculated by applying the activation function over the net input.

Output = function (net input calculated)

$$Y = F(Y_{in}) \qquad (1.3)$$

Similarities between artificial neural network and biological neural network based on the terminology used in them are shown in Table 1.

Processing of ANN depends upon:

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- Network Topology,
- Adjustments of weight or learning, and
- Activation function.

Table 1: BNN and ANN terminologies

Biological Neural Network (BNN)	Artificial Neural Network (ANN)
Soma	Node
Dendrites	Input
Synapse	Weights/ Interconnections
Axon	Output

5.2. Learning/ Adjustments of Weights

Learning, in artificial neural network, is the method of modifying the weights of connections between the neurons of a specified network. Learning in ANN can be classified into three categories namely supervised learning, unsupervised learning, and reinforcement learning.

- **Supervised Learning**: It is a dependent learning process which is done under a supervision of teacher. During the training of ANN under supervised learning, the input vector is given to the network, which will provide an output vector. On the basis of this error signal, the weights are adjusted until the actual output is matched with the desired output. Its block diagram is shown in Figure 2.

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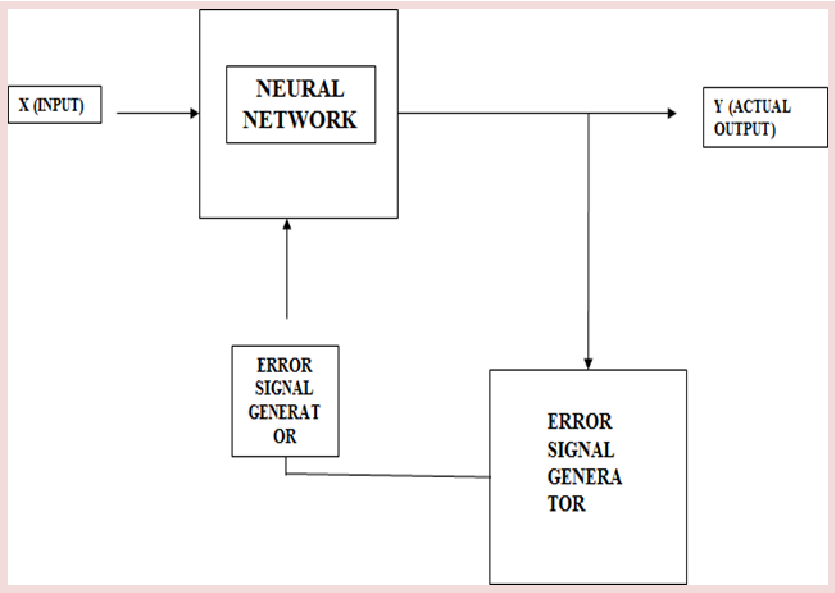

Figure 2: Supervised learning of ANN

- **Unsupervised Learning** : This type of learning is done without the supervision of a teacher and its process is independent. During the training of ANN under unsupervised learning, the input vectors of similar type are combined to form clusters. Hence, in this type of learning, the network itself must discover the patterns and features from the input data, and the relation for the input data over the output. Its block diagram is shown in Figure 3.

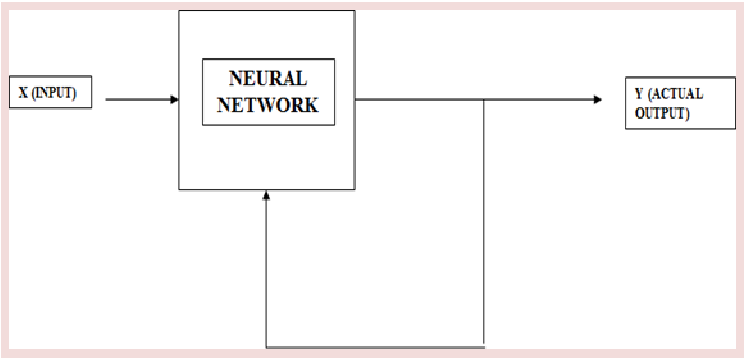

Figure 3: Unsupervised learning of ANN

- **Reinforcement Learning:** This type of learning is used to reinforce or strengthen the network over some critic information. This learning process is similar to supervised learning, however we might have very less information. During the training of network

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under reinforcement learning, the network receives some feedback from the environment. This makes it somewhat similar to supervised learning. Its block diagram is shown in Figure 4.

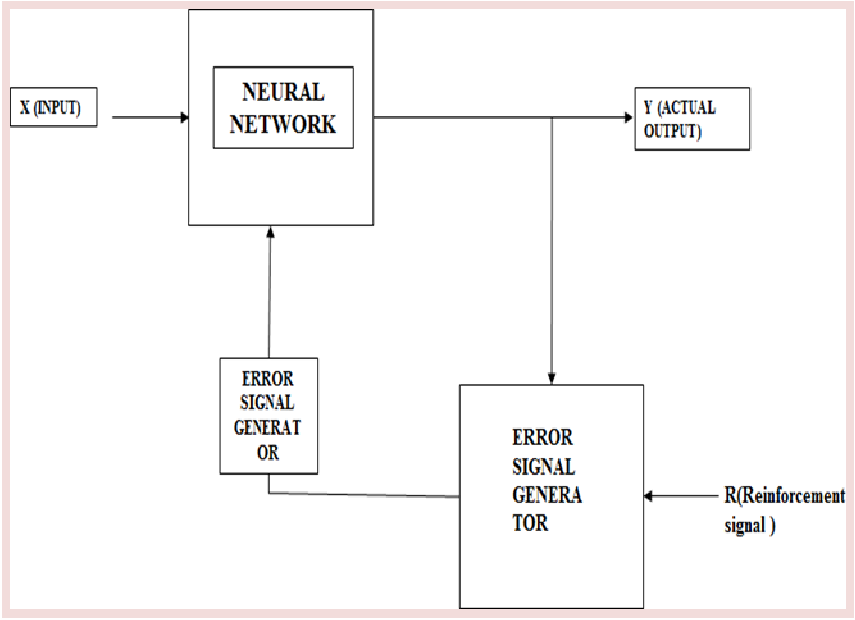

Figure 4: Reinforcement learning of ANN

5.3. GENETIC ALGORITHM

The biological analogy for genetic algorithms is the evolution of the species by survival of the fittest among consecutive generation for solving a problem. Each generation consist of a population of a character strings that are analogues to chromosomes that we see in our DNA. In a population, a new individual is generated by the crossover of the genetic information of two parents [12]. A genetic algorithm (GA) tries to simulate the natural evolution process. Its purpose is to optimize a set of parameters. Genetic algorithms are a class of parallel adaptive search algorithms based on the mechanics of natural selection and natural genetic system. It is capable of quickly finding the near global optimal solution in large solution space [13].. The algorithm terminates when the terminal condition met, terminal condition can be maximum number of generations, fitness limit, maximum time limit etc. [16].

- **Reproduction:** It is a process in which individual strings are copied according to their fitness. Whose fitness value is more that is having more chances to survive in next generation.

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- **Crossover:** is a process that can be divided in two steps. First, pairs of bit strings will be mated randomly to become the parents of two new bit strings. The second part consists of choosing a place (crossover site) in the bit string and exchanges all characters of the parents after that point. The process tries to artificially reproduce the mating process where the DNA of two parents determines the DNA for the newly born.
- **Mutation:** Even if previous process of reproduction and recombination are sufficient, mutation is included because the probability that a certain bit can't be changed by the previous operations due to its absence from the generation, either by a random chance or because it has been discarded.

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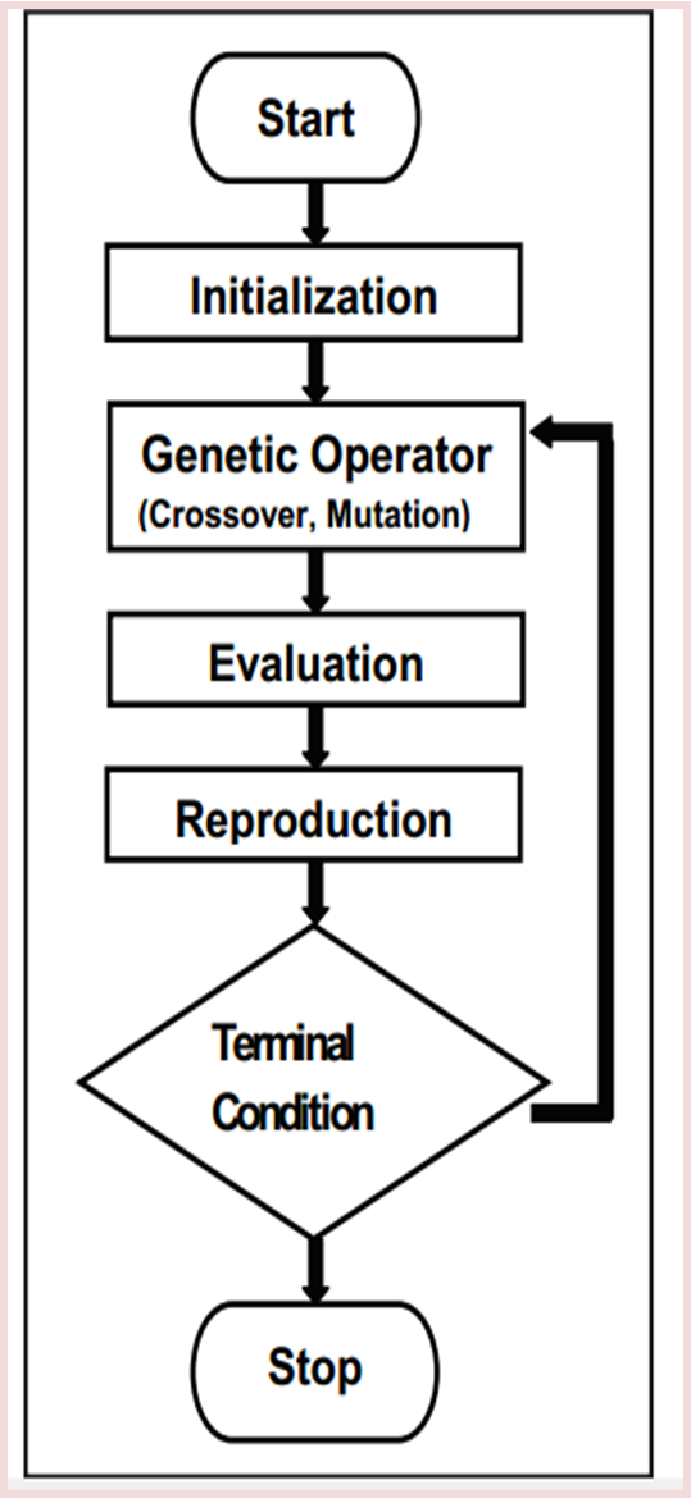

Figure 1.10: Flowchart of a generalised genetic algorithm

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5.4. HYBRID OF GA AND BP

In supportive approach GA and BP is independently applied to two different stages of the problem. The most common combination for this approach is to use a GA to pre-process the data set that is used to train a NN. In collaborative approach evolutionary algorithms and neural networks are used in a single system to evolve a population of neural networks best suited for a given task. In the combining process, the genetic algorithm is used to train the neural network. In this project genetic algorithm is used to define optimized initial weight for starting of BP thus the optimized back-propagation network has better accuracy and less training time than the standard back-propagation network.

Combination of neural network with evolutionary algorithms leads to evolutionary artificial neural networks (EANNs). Evolutionary algorithms like the GA is used to train neural nets, choose their structure or design the function of their neurons. In this project, genetic algorithms used to optimize the weights of neural network:

- Using GA to Train Neural Network: GA will train the network no matter how it is connected, whether it's a feed-forward or a feedback network. It can also train general networks which are a mixture of the two types.

(i) Creating a string or chromosome from simple neural network: All the weights in the network are joined to make one string. This string is then used in the GA as a member of the population. Each string represents the weights of a complete network.

(ii) Evaluating Fitness: Fitness is measured by calculating the error

$$Error = (target - output) \tag{1.6}$$

$$Fitness = \frac{1}{error} \tag{1.7}$$

The lower the error the higher the fitness.

Member with the highest fitness is selected as the optimized weights for neural network.

Conclusion

This study helps in the context of a set of desirable characteristics to evaluate different methods in this series and it reveals the strengths and weaknesses of various approaches. This paper gives a clear observation that no single method has all the desirable characteristics that a diagnostic system has. It is our view that some of these methods can transform each other into better diagnostic systems. Integrating these complementary features is one way to develop hybrid systems that can cross the boundaries of individual solution strategies. All studies conclude that ANN plays an important role in analog circuit fault detection**.** NN based GA method to detect faults in analog circuit is proposed and experimental validations have been carried out on state variable filter circuit. To enhance the performance of neural network and to overcome its limitations, initial weights of neural network are optimized using genetic algorithm. Neural network is optimized by using different parameters of genetic algorithm and performance of the different models of neural network has been compared to the back-propagation neural network and also compared to the neural network optimized by default parameters of genetic algorithm.

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